

FIG. 1
(RELATED ART)

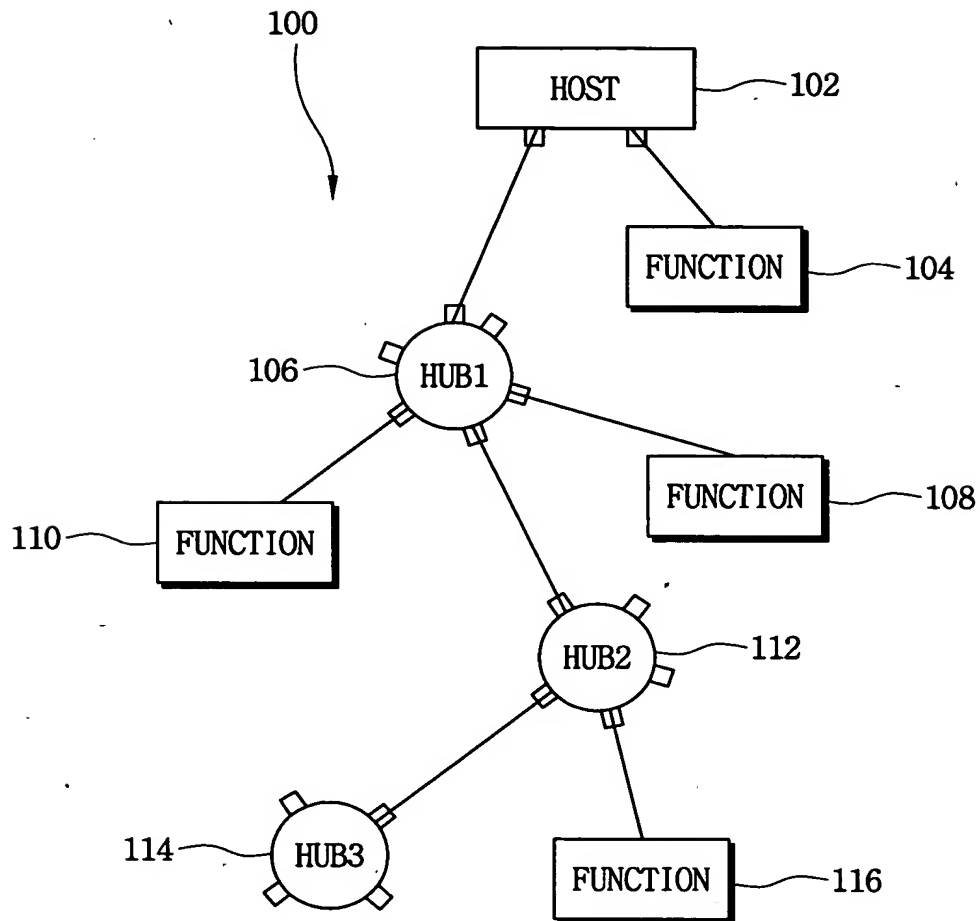


FIG. 2
(RELATED ART)

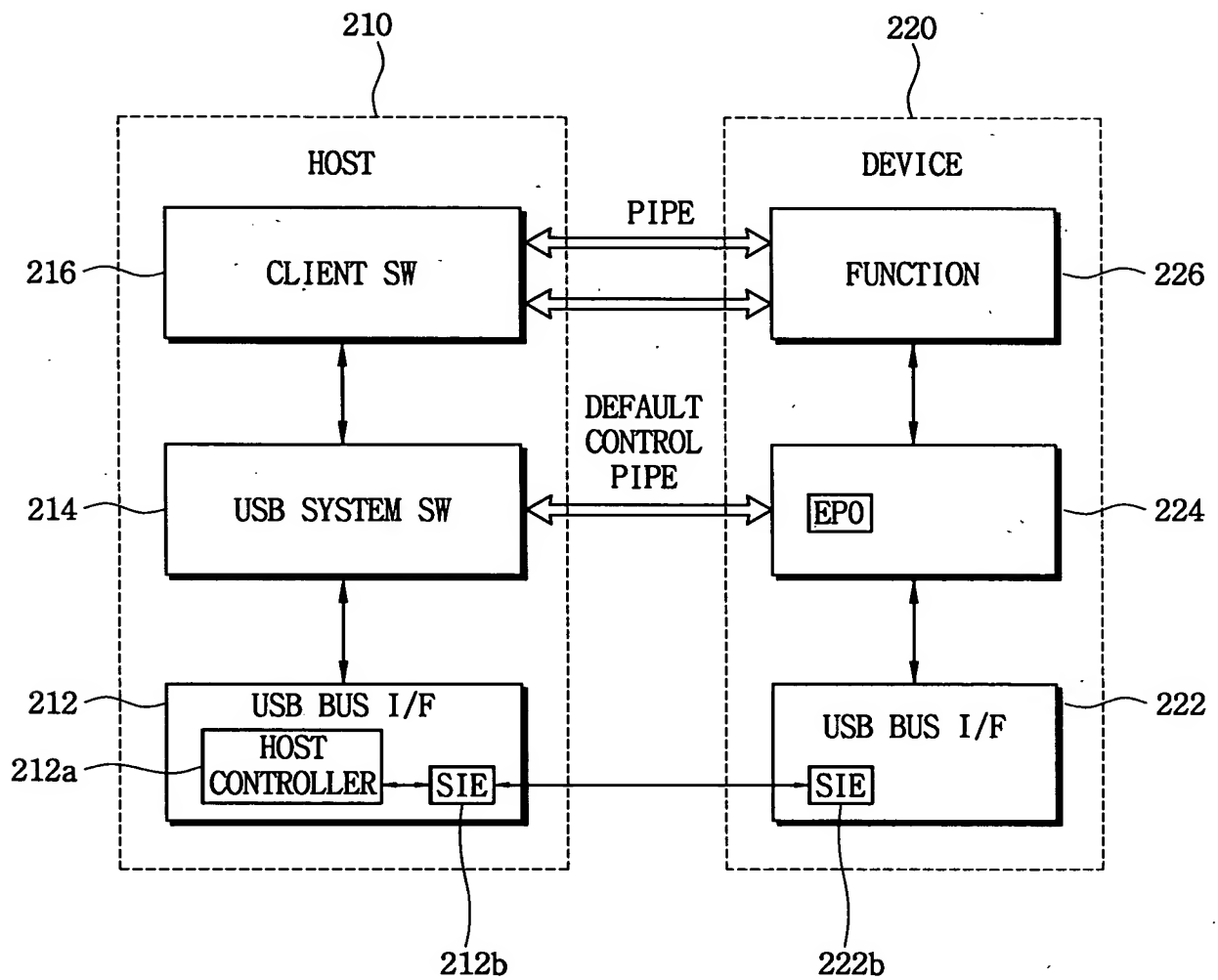


FIG. 3
(RELATED ART)

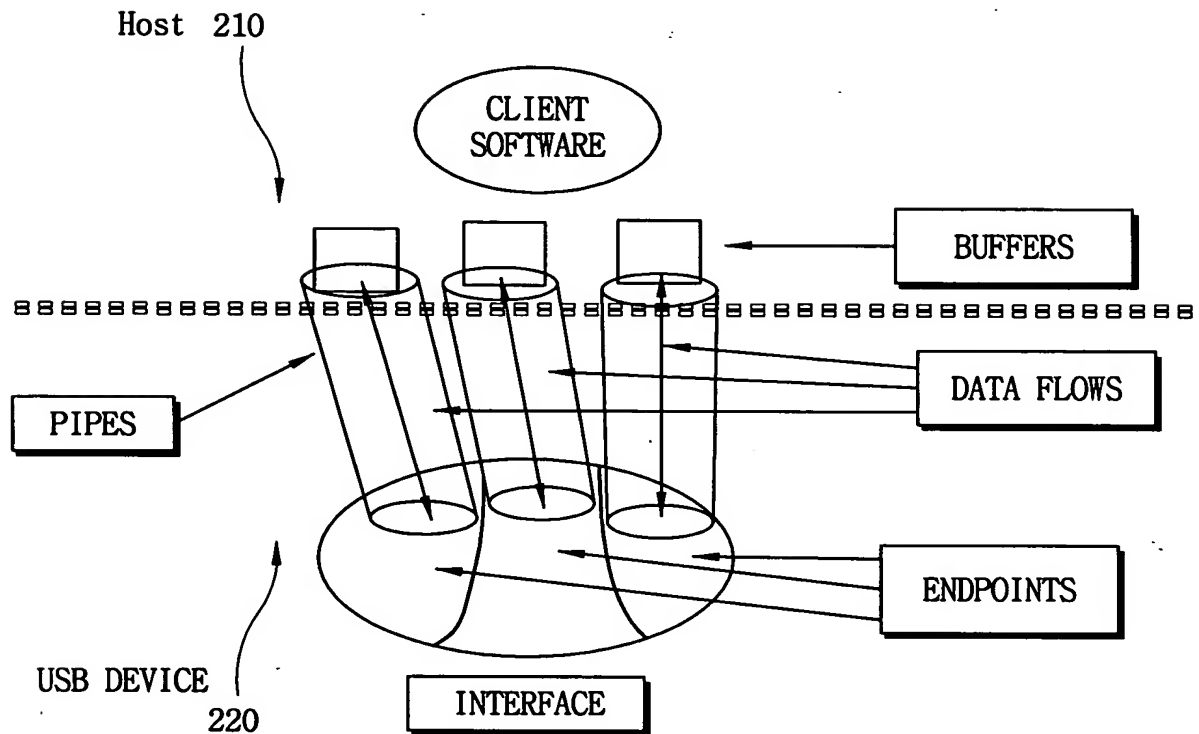


FIG. 4A
(RELATED ART)

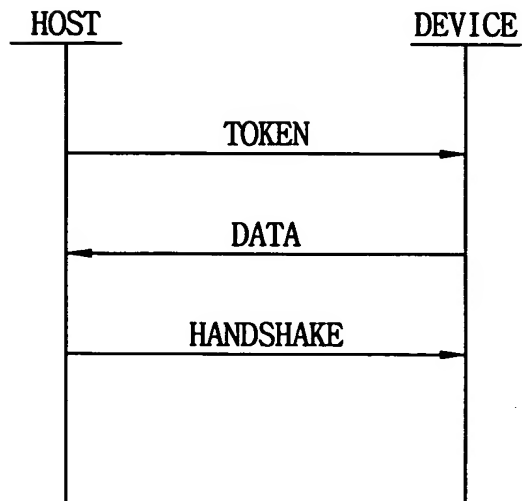


FIG. 4B
(RELATED ART)

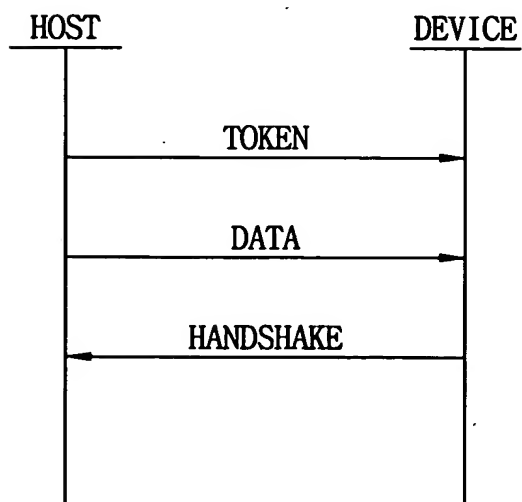


FIG. 5A
(RELATED ART)

FIELD	PID	ADDR	ENDP	CRC5
BIT	8	7	4	5

502

FIG. 5B
(RELATED ART)

FIELD	PID	FRAME NUM	CRC5
BIT	8	11	5

504

FIG. 5C
(RELATED ART)

FIELD	PID	DATA	CRC16
BIT	8	0-8192	16

506

FIG. 5D
(RELATED ART)

FIELD	PID
BIT	8

508

FIG. 6
(RELATED ART)

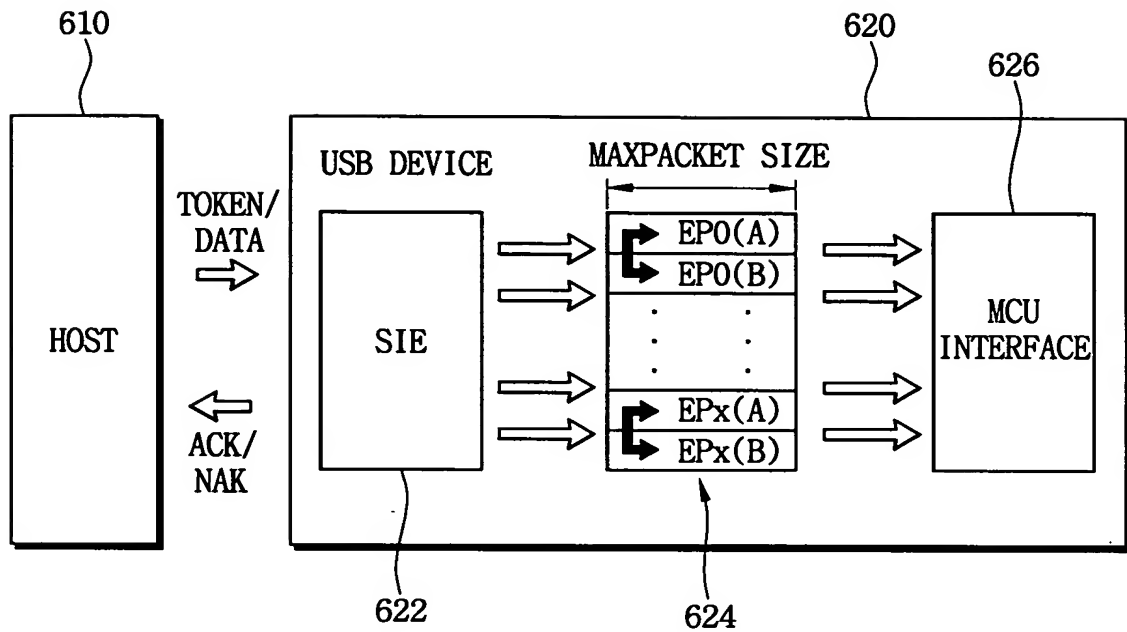


FIG. 7

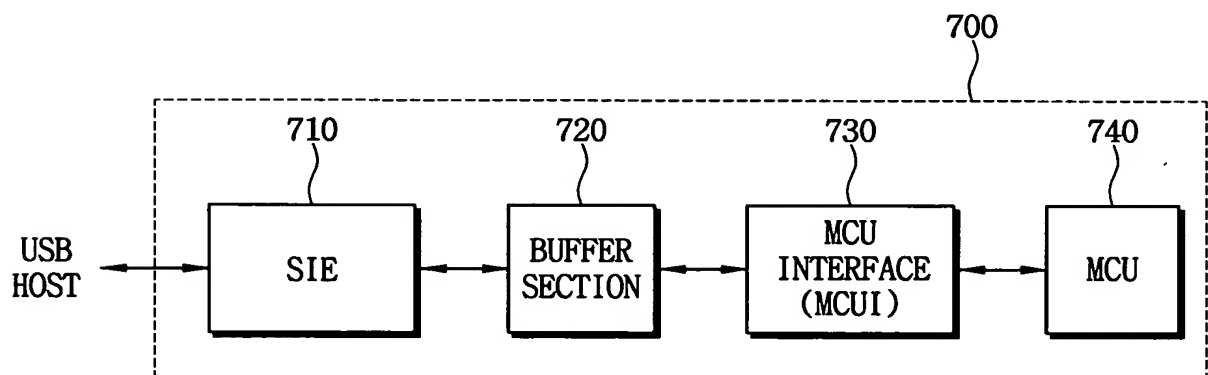


FIG. 8

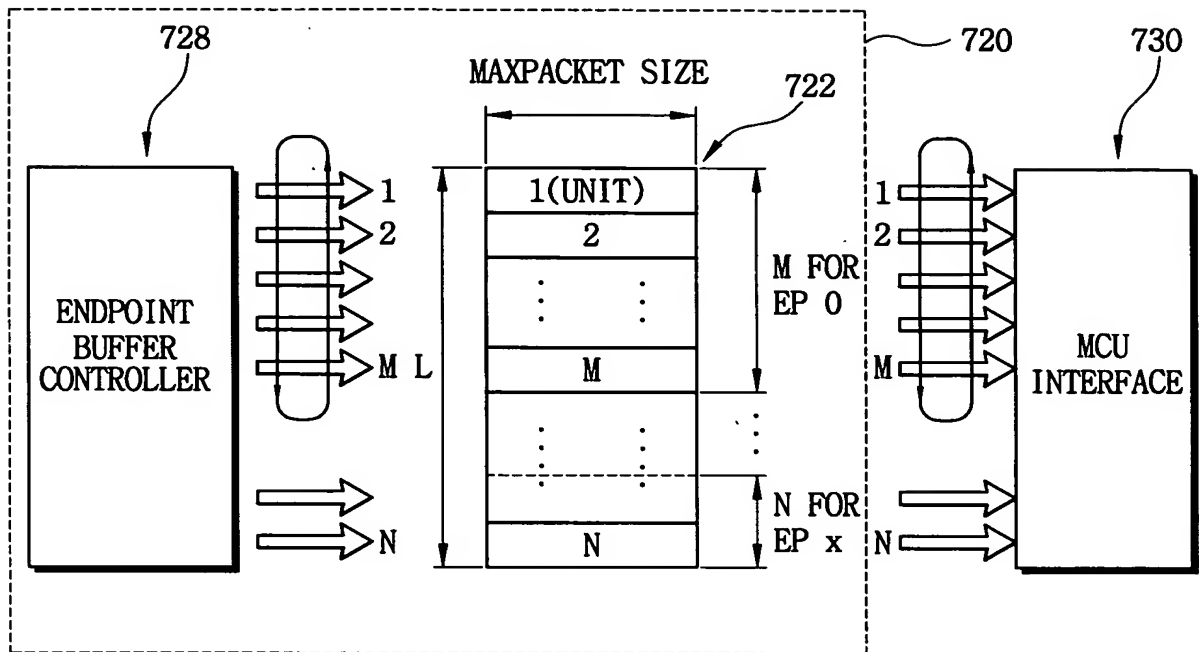


FIG. 9

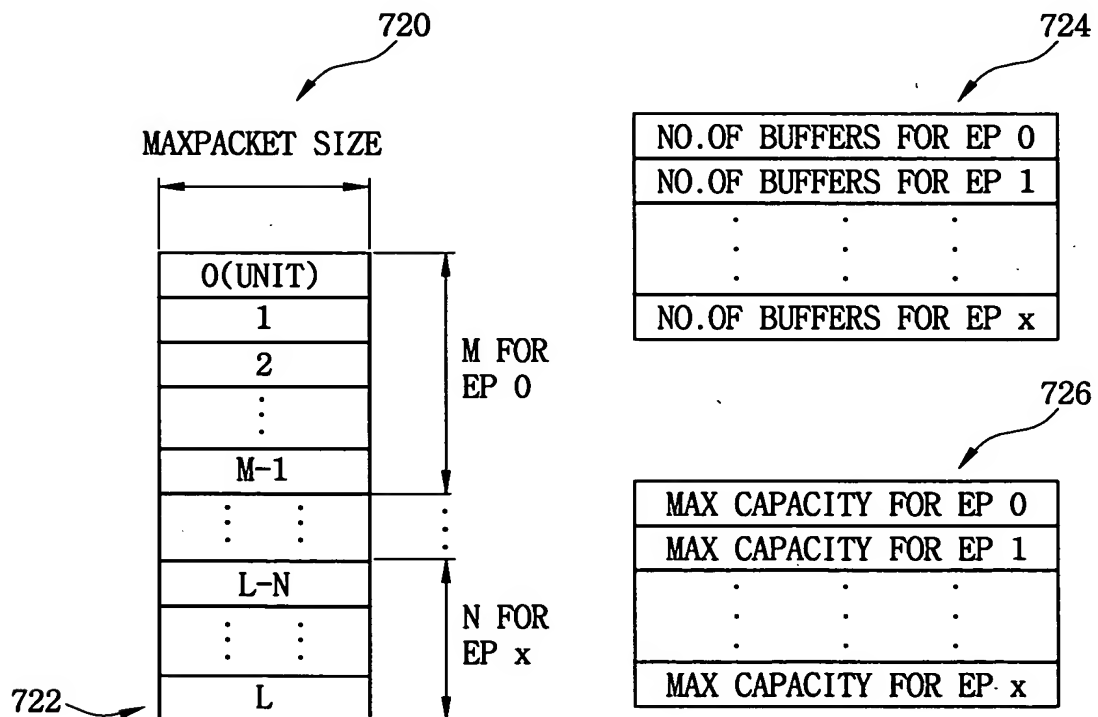


FIG. 10

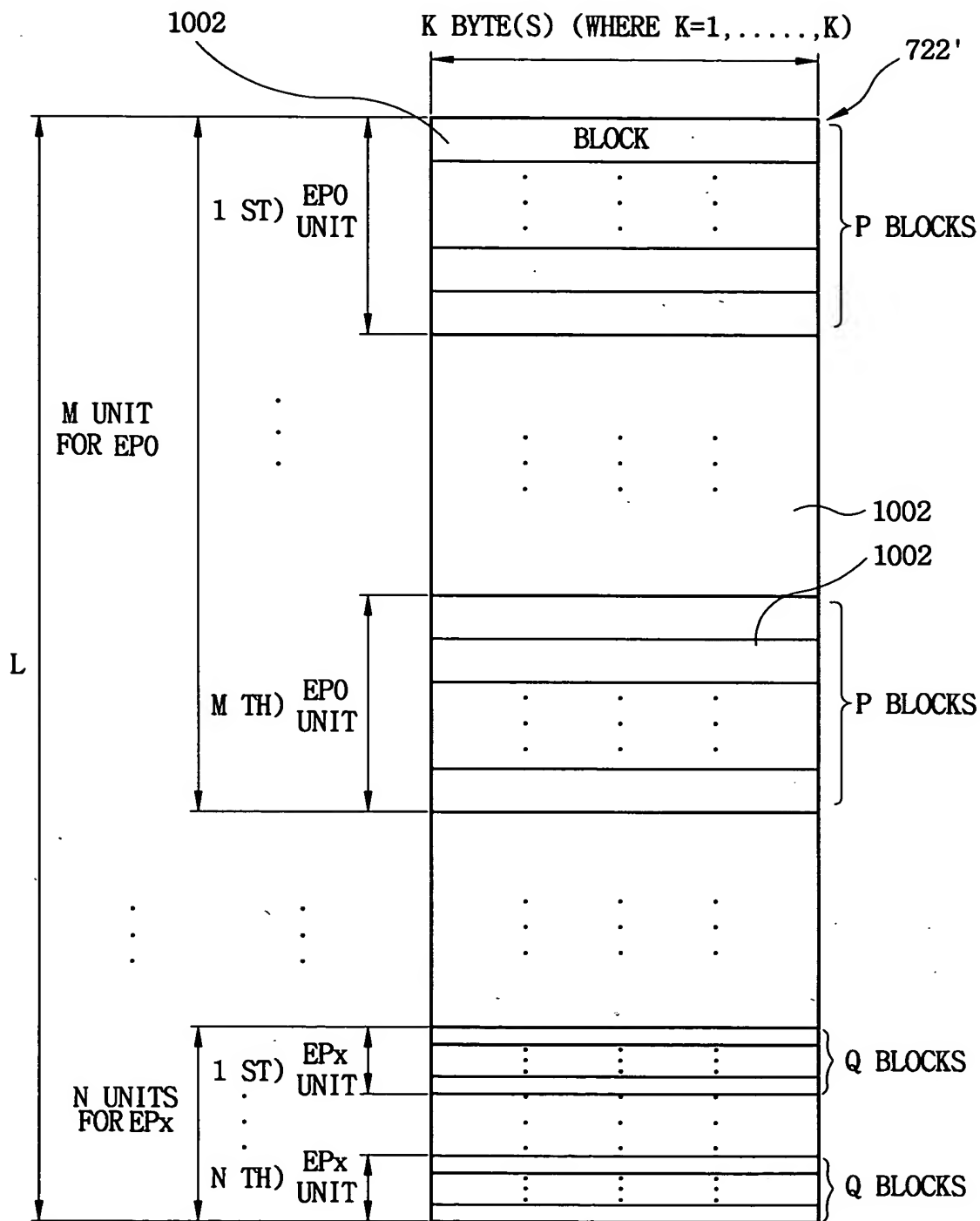
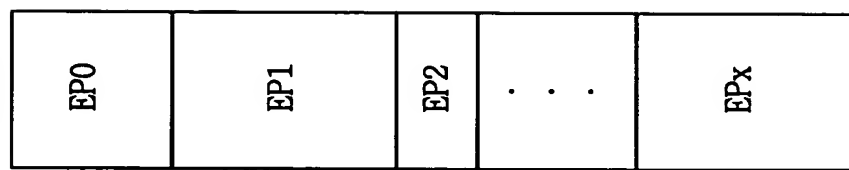


FIG. 11

INTERRUPT
TO
MCU

728

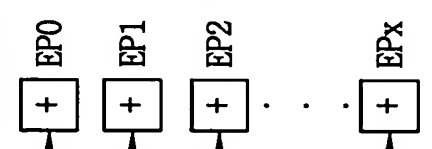
PROGRAMMABLE
ENDPOINT
FIFO



NAK
THRESHOLD
CONTROLLER

820

N-BIT NAK
COUNTERS



THRESHOLD
VALUES

POINTER
CONTROL
SECTION

EP0
POINTER
EP1
POINTER
EP2
POINTER
...
EPx
POINTER

830

M-BIT PERIOD
CONTROLLABLE
TIMER

840

FIFO STATUS

810

NAK TO "SIE"

722

FIG. 12

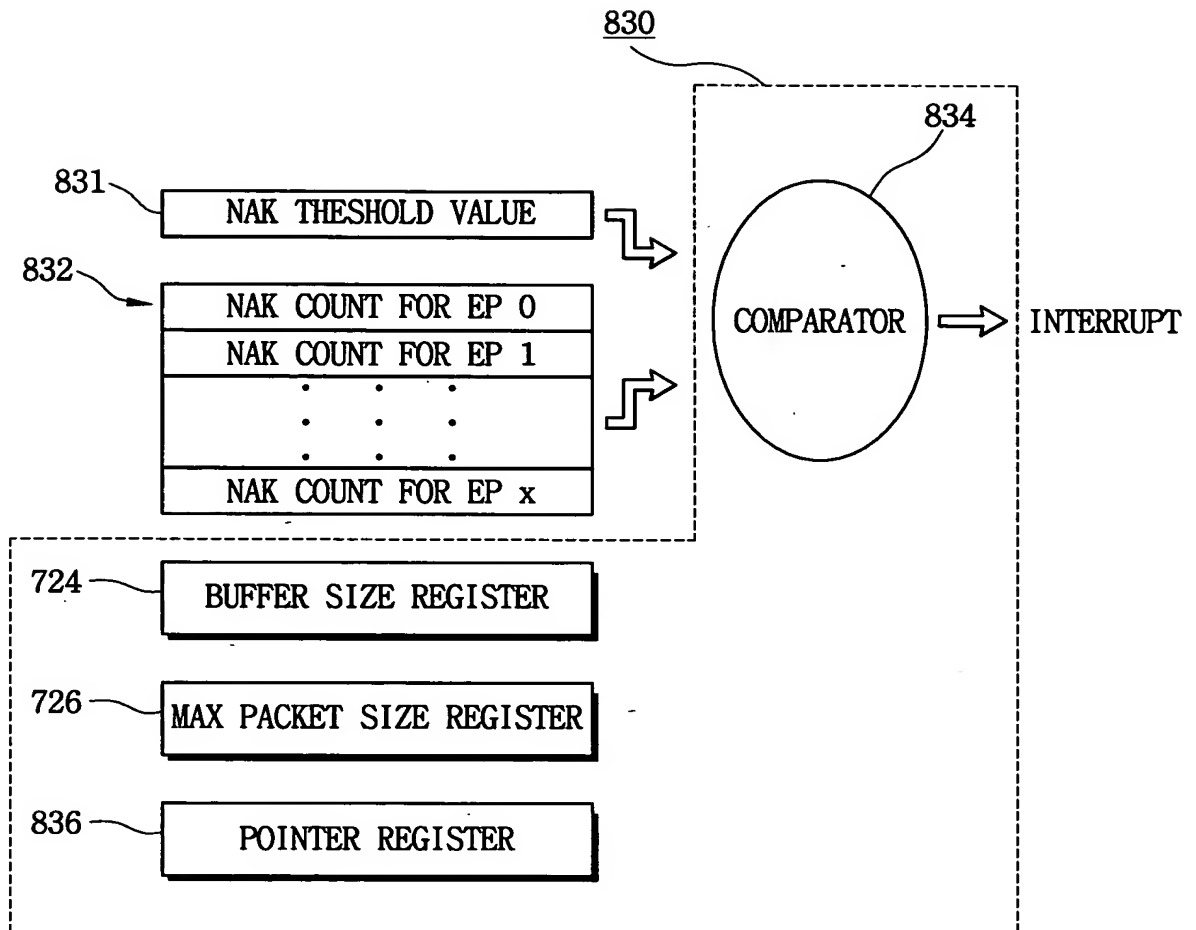


FIG. 13

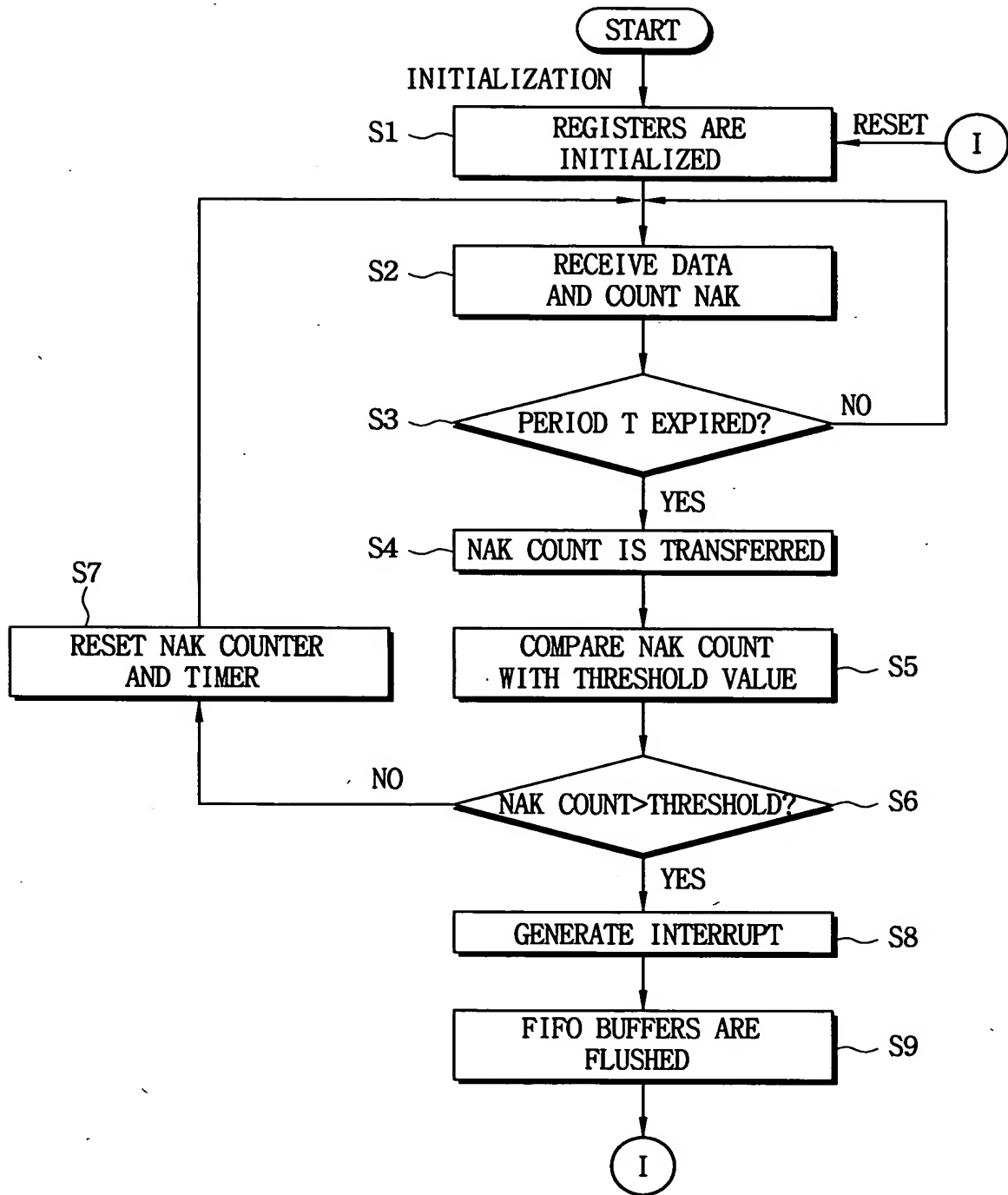


FIG. 14

